Implementation and Evaluation of Single Stage Transistor Amplifiers.

Design and Analysis of Single Stage Amplifers Using MOSFET and BJT.

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***Abstract*—This paper presents the design and implementation of single-stage transistor amplifiers using a common source (CS) metal oxide field effect transistor (MOSFET) and a common emitter (CE) bipolar junction transistor (BJT). Leveraging MOSFET parameters extracted from experimental data and calculated BJT characteristics, the amplifiers are analyzed and constructed to reinforce theoretical concepts. Performance comparisons highlight the advantages, limitations, and tradeoffs between the two semiconductor devices, emphasizing their roles in amplifier design and signal processing applications.**

I. Introduction

The evolution of semiconductor devices has profoundly shaped modern electronics, enabling compact, efficient, and high-performance systems. Among these devices, the Bipolar Junction Transistor (BJT) and the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) stand out as foundational components in analog and digital circuit design. [1] The BJT, introduced in 1947 by John Bardeen, Walter Brattain, and William Shockley at Bell Labs, marked a pivotal shift from bulky vacuum tubes to solid-state electronics. A decade later, the MOSFET emerged from the work of Mohamed Atalla and Dawon Kahng, also at Bell Labs, offering a voltage-controlled alternative with superior scalability and power efficiency.

This experiment builds upon theoretical principles explored in electronic circuits courses by designing and analyzing two single-stage amplifiers: a Common Emitter (CE) amplifier using a BJT and a Common Source (CS) amplifier using an N-type MOSFET. By leveraging experimentally derived MOSFET parameters and calculated BJT characteristics, the amplifiers are constructed and evaluated to highlight their respective performance traits and design tradeoffs. This hands-on approach reinforces key concepts in semiconductor physics and amplifier design, bridging the gap between theory and practical implementation.

II. MOSFET Parameters & Simulation

For our hardware component, we will be utilizing the 2N7000 N-type MOSFET. A critical part of our design process involves determining the transconductance parameter, (K_n), and the threshold voltage (V_T) of the device. The threshold voltage signifies the minimum gate-to-source voltage (V_{GS}) required to form a conductive channel between the source and drain terminals-effectively turning the transistor "on". Accurately identifying this parameter is essential for predicting the onset of conduction.

To characterize the transistor, we first perform a DC voltage sweep using NI Multisim. This simulation allows us to analyze the drain current (I_D) behavior as V_{GS} varies from 0 to 3V.

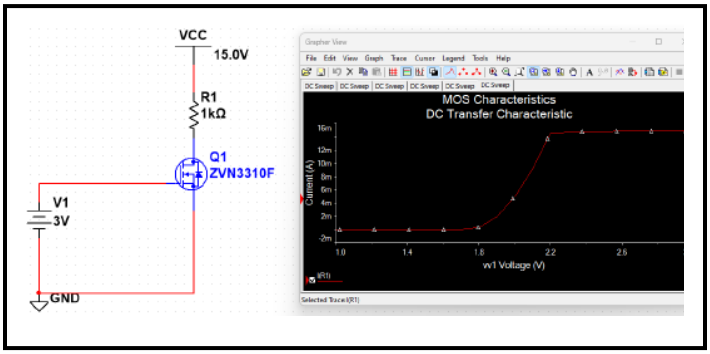

Fig. 1 N-MOS DC Sweep Simulation Results.

The results of the sweep provided insight into the transistor's turn-on characteristics. To verify the simulation, a physical circuit was constructed mirroring the simulated topology. The gate voltage was incremented, and the resulting drain current values were recorded as follows:

Input Voltage (V)	Output Voltage (V)	Output Current (mA)
0	14.96	0.04
0.5	14.96	0.04
1	14.56	0.44
1.05	14.18	0.82
1.1	13.59	1.41
1.15	12.85	2.15
1.2	11.7	3.3
1.25	10.33	4.67
1.3	8.53	6.47
1.35	6.48	8.52
1.4	4.23	10.77
1.45	2.04	12.96
1.5	0.484	14.516
1.55	0.273	14.727
1.6	0.223	14.777
1.65	0.194	14.806
1.7	0.175	14.825
1.75	0.161	14.839
1.8	0.15	14.85
1.85	0.142	14.858
1.9	0.135	14.865
1.95	0.128	14.872
2	0.122	14.878
2.05	0.117	14.883
2.1	0.112	14.888
2.15	0.106	14.894
2.2	0.101	14.899
2.25	0.096	14.904
2.3	0.092	14.908
2.35	0.088	14.912
2.4	0.084	14.916
2.45	0.081	14.919
2.5	0.078	14.922
3	0.061	14.939
3.5	0.053	14.947
4	0.049	14.951

Fig. 2 N-MOS incremented Hardware Measurements.

Using these tabulated values, we can create a characteristic curve of our I_D and compare these results against our simulation.

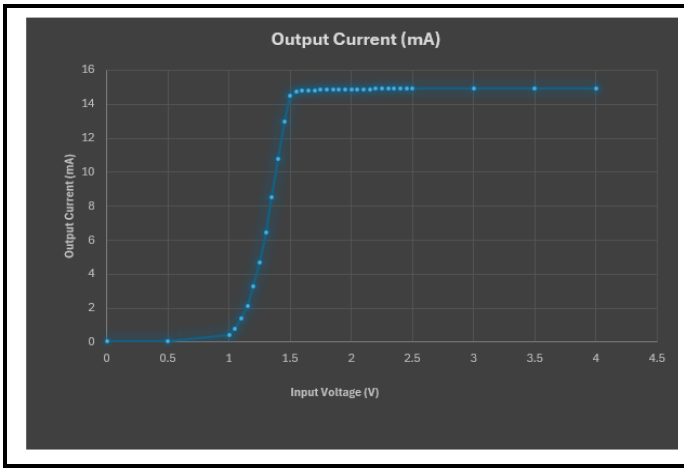

Fig. 3 N-MOS DC Sweep Hardware Results.

The correspondence between the simulated and hardware data validates our model and supports the quadratic expression for saturation-region drain current:

$$I_D = \frac{1}{2}K_n(V_{GS} - V_T)^2 \qquad (1)$$

Now that we have accurately captured the behavior of I_D as we ranged V_{GS} we can use equation one applied to two data points to solve for our unknowns:

$$I_{D1} = \frac{1}{2}K_n(V_{GS} - V_T)^2 \, , I_{D2} = \frac{1}{2}K_n(V_{GS} - V_T)^2$$

$$0.0033A = \frac{1}{2}K_n(1.2 - V_T)^2 \, , 0.00467A = \frac{1}{2}K_n(1.25 - V_T)^2$$

$$K_n = \frac{0.0066}{1.44 - 2.4V_T + V_T^2}$$

$$0.00934 = \frac{0.0066}{1.44 - 2.4V_T + V_T^2}(1.25 - V_T)^2$$

$$0.0134 - 0.0224V_T + 0.00934V_T^2 = 0.0066(1.56 - 2.5V_T + V_T^2)$$

$$0.0134 - 0.0224V_T + 0.00934V_T^2 = 0.0103 - 0.0165V_T + 0.0066V_T^2$$

$$0.0031\text{-}0.00592V_T + 0.00274V_T^2 = 0$$

$$V_T = 1.12V \text{ or } 0.768V$$

Solving the quadratic equation above provides two solutions. Based on the plot in figure 3, we select the 0.77V to be more accurate. Substituting this back

into equation one, we can solve for our transconductance value.

$$K_n = \frac{0.0066}{1.44-2.4V_T+V_T^2} = \frac{0.0066}{1.44-2.4(0.77)+0.77^2} = \frac{35.7mA}{V^2}$$

$$K_n = \frac{35.7mA}{V^2}, \qquad V_T = 0.77\text{V}$$

Now that we have our transconductance parameter and threshold voltage, we can now design a single stage amplifier with the given specifications: V_D = 5V, I_D = 1mA, and V_G = 0v. We can use our design specifications to solve our drain and source resistors using the following equations.

$$I_D = \frac{1}{2}K_n(V_{GS} - V_T)^2 \text{ (Device Equation)} \quad (2)$$

$$0 = V_{GS} + I_D R_S - 15 \text{ (Input Equation)} \quad (3)$$

$$V_D = 15 - I_D R_D \text{ (Output Equation)} \quad (4)$$

Using equation 2 to solve for our V_{GS}:

$$1mA = \frac{35.7mA}{2V^2}(V_{GS} - 0.77)^2$$

$$0.056 = (V_{GS} - 0.77)^2$$

$$\sqrt{0.056} + 0.77 = V_{GS}$$

$$V_{GS} = 1.007\text{V}$$

Now that we have V_{GS} we can solve our drain resistance (R_D) and source resistance (R_S) as follows:

$$R_S = \frac{15 - V_{GS}}{I_D} = \frac{15 - 1.007}{1mA} = 13.993K\Omega \approx 14K\Omega$$

We can also see:

$$R_D = \frac{15 - V_D}{I_D} = \frac{15 - 10}{1mA} = 10K\Omega$$

We don't have a 14KΩ resistor readily available, but we can use a 47KΩ and 10KΩ resistor in parallel. We can prove this as follows:

$$R_S = 47K||10K = \frac{47 * 10}{47 + 10} = 14.03K\Omega$$

Having solved our resistance values, we can solve for I_D and V_D to ensure we are still meeting our design tolerances:

$$I_D = \frac{15 - V_{GS}}{R_S} = \frac{15 - 1.007}{14.03K\Omega} = 0.997mA$$

$$V_D = 15 - I_D R_D = 15 - (0.997)(10) = 5.03V$$

We can see from our above calculations; we have met our design specifications with an approximate error of 0.45%. Now that we have all of our component values, we can determine the gain of our amplifier using our following gain equation:

$$V_{OUT} = R_D(g_m V_{GS}) \quad (5)$$

$$A_V = \frac{V_{OUT}}{V_{GS}} = R_D g_m$$

We know that the transconductance (g_m) is given by:

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

Putting this into our gain equation:

$$A_V = R_D\left(\frac{2I_D}{V_{GS} - V_T}\right) = 10K\left(\frac{2 * 0.997mA}{1.007 - .077}\right)$$

$$A_V = -84.14\,{}^{v}/_{v}$$

Thus, the designed amplifier achieves a voltage gain of -84.14 satisfying the initial requirements. The design is now ready for simulation and physical testing.

III. N-MOS Single Stage Amplifier

Following the analytical design of the common-source amplifier, the circuit was simulated using NI Multisim 14.3 to validate the calculated parameters. This simulation allowed for the observation of expected circuit behavior prior to physical implementation, ensuring both performance accuracy and circuit safety. While also verifying our gain of $4V_{P\text{-}P}$. The simulation schematic can be seen in figure 4 below:

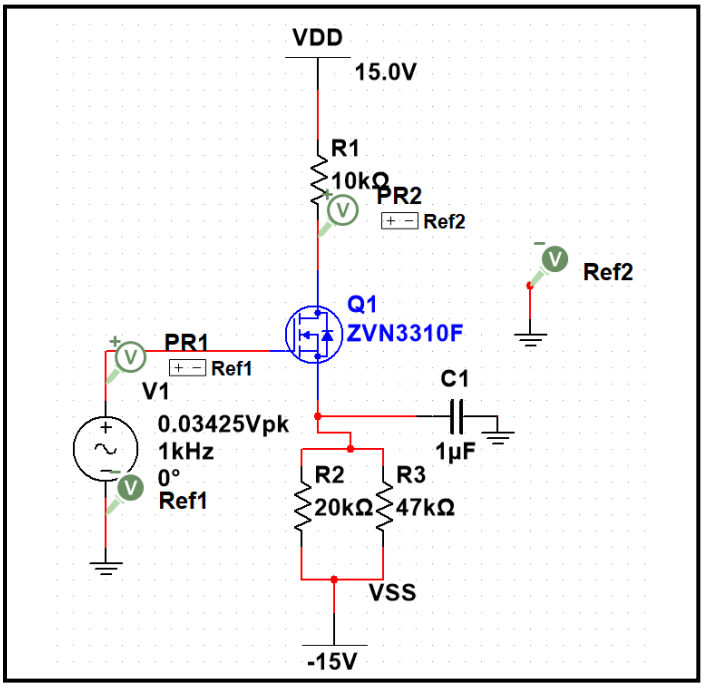

Fig. 4 N-MOS Common Source Amplifier Simulation Circuit.

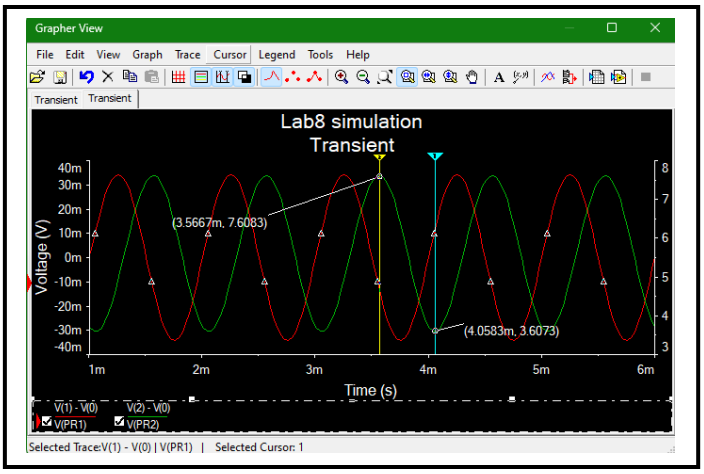

Fig. 5 Simulation results as seen on Oscilloscope.

From the oscilloscope output in figure 5, we can see that we were successfully able to simulate an output voltage of $4.001V_{P\text{-}P}$. Performing our gain calculation (Vo/Vi), we can see we have a simulated gain of -58.41V/V. This result is expected, as we must consider the high impedance of the capacitor. Recall that the impedance of a capacitor is measured as follows:

$$X_c = \frac{1}{2\pi f C} \qquad (6)$$

We can see from equation 6 that as our frequency (f) increases, the impedance from the capacitor decreases. This is expected behavior of a capacitor because it's acting as a filter for lower frequencies. Noting that we have a higher impedance at 1KHz, we should expect a much closer gain to our calculations when we increase our frequency to 10KHz.

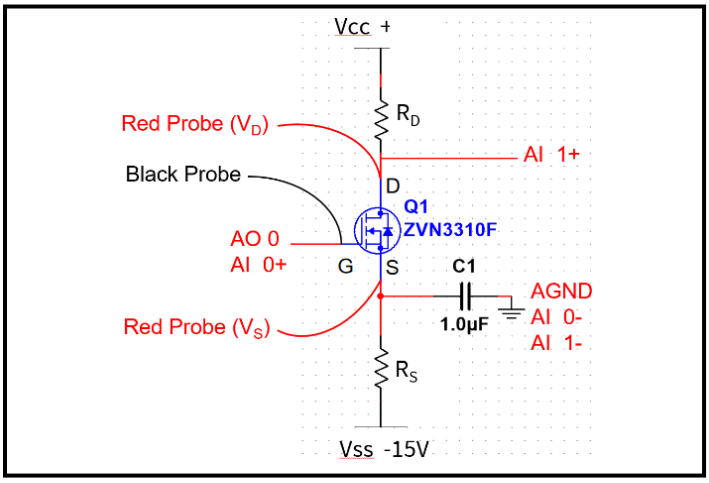

Fig. 6 N-MOS Hardware circuit wiring diagram.

In our hardware implementation we will be using the 2N7000(N-MOS) transistor. Noting the orientation of the Drain and Source, we first connect the Drain node across R_D to V_{CC}. Next, we connect the source node across R_S to V_{SS}. The capacitor is added to the circuit and the hardware connection can be seen in figure 6. Once the circuit is physically connected, the DC voltage is measured at V_S and V_D. This is done using the multimeter with the NI myDAQ. Then our 0.08VP-P 1KHz sinusoidal input is applied to the Gate. The input and output waveform are then seen on the oscilloscope. This is then repeated for a frequency of 10KHz. Once the results on the oscilloscope are recorded, the gain of our amplifier can be calculated.

Measured vs Calculated Common Source Amplifier Results.

	Measured	**Calculated**	**Percent error**
V_D	4.91V	5.03V	2.39%
V_S	-1.105V	-1.007V	8.87%
I_D	0.99mA	0.997mA	0.7%
A_V (f =1KHz) 0.08V_{PP}	-49.89V/V	Simulated (-58.41) V/V	14.59%
A_V (f = 10KHz) 0.05V_{PP}	-85.16V/V	-84.14V/V	1.19%

Fig. 7 Tabulated Common Source Amplifier results.

We can note from our Oscilloscope that our output is $3.991V_{P\text{-}P}$ for 1KHz, and our output is $4.252V_{P\text{-}P}$ at 10Khz. This is what we expect from our circuit as we are looking for $4V_{P\text{-}P}$ output. The reason we can see a slight deviation from our simulated results is because we only have a 2 decimal point adjustment on the NI myDAQ function generator. If our equipment tolerance was higher, we could achieve a closer output amplitude, but for our purposes this is ample. We can also see from the above tabulated results in figure 7 that almost all our values are within range. The only value with a larger percentage error is our gain at 1KHz. This discrepancy is most likely due to the impedance from the capacitor as we discussed earlier. We can see that when we increase the frequency to 10KHz we are much closer to our calculated gain. This is because when we increase the frequency, we in turn also decrease the impedance

across the capacitor. Overall, our results concur with our calculations, and we were able to meet our design specifications of creating a single stage Common Source Amplifier with a VD ≈ 5V, and an ID ≈ 1mA.

IV. BJT Amplifier Calculations and Design

To complement the MOSFET-based amplifier, we designed a single-stage common-emitter amplifier utilizing a Bipolar Junction Transistor (BJT) based on the following design specifications: A desired collector current (I_C) = 1mA, collector voltage (V_C) = 7V, and V_B = 5V. It's also important to note for our calculations to assume a very high β. Given that R_1 should be in the tens of kilo-ohms, we can let R_1 be 10KΩ. Solving for R_2:

$$V_B = \frac{R_2}{(R_2 + R_1)} * V_{CC}$$
$$\frac{5}{15}(R_2 + 10K) = R_2$$
$$R_2 = 5K\Omega$$

Seeing that we have 5KΩ, we can use two 10KΩ resistors in parallel for R_2. Next, we can solve for R_3. Since we can assume β to be very high, we can see that $I_C \approx I_E$. This is because

$$I_C = \frac{\beta}{\beta + 1} * I_E$$

Since β is a large value $\frac{\beta}{\beta+1} \approx 1$ Therefore we can see that $I_C \approx I_E$. Using this, we can now solve for R_3 as follows:

$$V_C = V_{CC} - I_C R_3$$
$$\frac{15 - 7}{1mA} = R_3$$
$$R_3 = 8K\Omega$$

In our components, we do not have an 8KΩ, but we do have a 47KΩ and a 10KΩ resistor. As we can see by the following calculation, if we add these in parallel, we get our required R_3 value:

$$R_3 = 47K\Omega||10\text{K}\Omega = \frac{47 * 10}{10 + 47} = 8.246K\Omega \approx 8\text{K}\Omega$$

Since we know that we want a gain of our amplifier to be A_V = -10V/V, we can use our calculated R_3 value to solve the following equation for R_4:

$$Gain = -\frac{R_3}{R_4}$$
$$R_4 = \frac{-R_3}{Gain} = \frac{-8K}{-10} = 800\Omega$$
$$R_4 = 800\Omega$$

Again, we can use a parallel combination of 4.7KΩ and 1KΩ to achieve our desired resistance:

$$R_4 = 4.7K\Omega||1\text{K}\Omega = \frac{4.7 * 1}{1 + 4.7} = 824.6\Omega \approx 800\Omega$$

Since we now know R_4, we can solve for R_5:

$$V_B = V_{BE} + I_E(R_4 + R_5)$$
$$\frac{5 - 0.7}{1mA} = (R_4 + R_5)$$
$$R_5 = 4.3K\Omega - .8K\Omega$$
$$R_5 = 3.5K\Omega$$

We can put two 6.8KΩ resistors in parallel to achieve this:

$$R_5 = 6.8K\Omega||6.8\text{K}\Omega = \frac{6.8 * 6.8}{6.8 + 6.8} = 3.4K\Omega \approx 3.5\text{K}\Omega$$

Now that we have obtained our resistor values for our designed amplifier, we can recalculate the current I_C and solve for our emitter voltage V_E:

$$R_{BB} = R_1||R_2 = \frac{10K * 5K}{10K + 5K} = 3.33K\Omega$$

$$V_{BB} = \left(\frac{R_2}{R_1 + R_2}\right) * V_{CC} = \left(\frac{5}{10 + 5}\right) * 15 = 5V$$

Given that we have solved for R_{BB} and V_{BB}, we can use these to create a Thevenin's equivalent of our amplifier circuit as seen below to then solve for I_C and V_E.

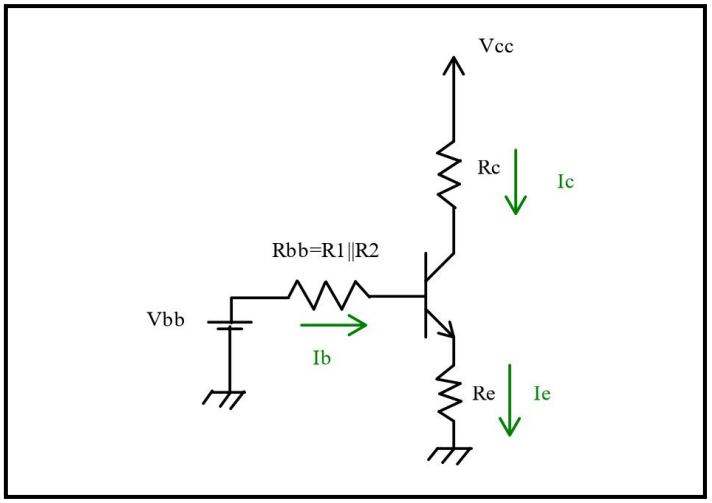

Fig. 8 Thevenin's Equivalent BJT Common Emitter Amplifier.

Since we now have our solvable circuit, we can develop a circuit equation to solve our values seen below. It's important to note that for our BJT Common Emitter amplifier we can assume $V_{BE} = 0.7V$ and that $I_E = (\beta+1)\, I_B$.

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E \qquad (7)$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_{BB}}{\beta + 1}}$$

$\frac{R_{BB}}{\beta+1}$ is 0 since β is very large,

$$I_E = \frac{5 - 0.7}{4.23K + 0} = 1.017mA$$

$$V_E = I_C R_E = 1.017mA * 4.23K\Omega = 3.3V$$

$I_C = \frac{\beta}{\beta+1} * I_E$, again, β is very large

$$I_C \approx I_E = 1.017mA$$

As we can see from our results, solving equation 7 we have successfully designed a common emitter amplifier such that $I_C \approx 1$mA. Using our solved values, we can now create a small signal equivalent AC circuit so that we can determine the gain of our amplifier.

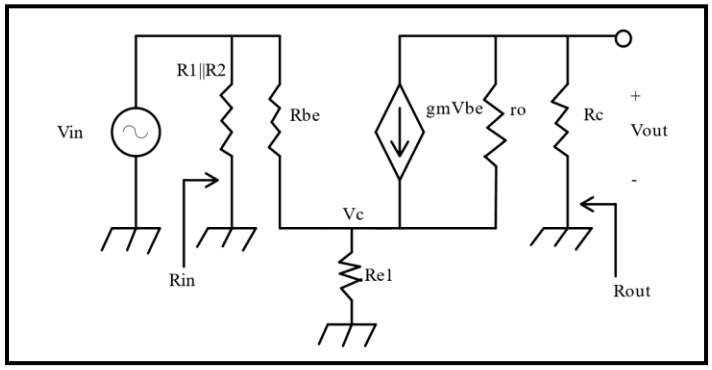

Fig. 9 AC Small Signal Equivalent BJT Common Emitter Amplifier.

Creating a node equation at V_{OUT} we can see the following, we can ignore r_o as we assume its large with respect to the external resistors:

$$\frac{V_O}{R_C} + g_m V_{BE} = 0, V_{BE} = \frac{-V_O}{g_m R_C}$$

$$V_{BE} = \frac{-V_O}{g_m R_C} \qquad (8)$$

Now creating a node equation at V_C:

$$\frac{V_E - V_B}{R_{BE}} + \frac{V_E}{R_{E1}} - g_m V_{BE} = 0$$

$$V_E = R_{E1}(g_m + \frac{1}{R_{BE}})V_{BE}$$

$$V_E = \frac{R_{E1}}{R_{BE}}(g_m R_{BE} + 1)V_{BE}$$

$$V_E = \frac{R_{E1}}{R_{BE}}(\beta + 1)V_{BE} \qquad (9)$$

Finally, we can create a node equation at V_B, otherwise known as V_{IN}, and we can combine equations 8 and 9 as follows to solve for the gain of our amplifier:

$$V_{IN} = V_{BE} + V_E$$

$$V_{IN} = [1 + \frac{R_{E1}}{R_{BE}}(\beta + 1)]V_{BE}$$

$$V_{IN} = \left(\frac{R_{BE} + (\beta + 1)R_{E1}}{R_{BE}}\right)\left(\frac{-V_O}{g_m R_C}\right)$$

$$A_V = \frac{V_o}{V_i} = -g_m R_C \left(\frac{R_{BE}}{R_{BE} + (\beta + 1)R_{E1}}\right)$$

We know that $g_m R_{BE} = \beta$ and that $(\beta + 1)R_{E1} \gg R_{BE}$

Therefore:

$$A_V = \frac{-g_m R_{BE} R_C}{(\beta + 1)R_{E1}} = \frac{\beta}{\beta + 1} * \frac{-R_C}{R_{E1}}$$

Again, since β is very large, we can assume that

$\frac{\beta}{\beta+1} = 1$, using this assumption we can finally calculate our gain as:

$$A_V = \frac{-R_C}{R_{E1}} = \frac{-8.25K\Omega}{825\Omega} = -10V/V$$

We can see after our calculations of our common emitter amplifier; we have successfully designed the BJT amplifier such that $I_C \approx 1mA$ and still has a gain of -10V/V based on the resistor values we have used. We were able to prove this using our small signal gain circuit and we can now begin simulating our amplifier.

V. BJT Simulation & Hardware Testing

After determining the required component values, NI Multisim was used to verify the design and simulate the behavior of the common-emitter amplifier. The simulation employed a supply voltage of V_{CC} = +15V, with resistor values—both series and parallel combinations—corresponding to R_1, R_2, R_C, R_{E1}, and R_{E2} as calculated.

The 2N3904 NPN BJT, functionally equivalent to the device available in the component kit, was selected for the simulation. Input and output AC probes were positioned appropriately to facilitate transient analysis. The sinusoidal input amplitude was gradually increased to achieve the target output of 4 V_{P-P}.

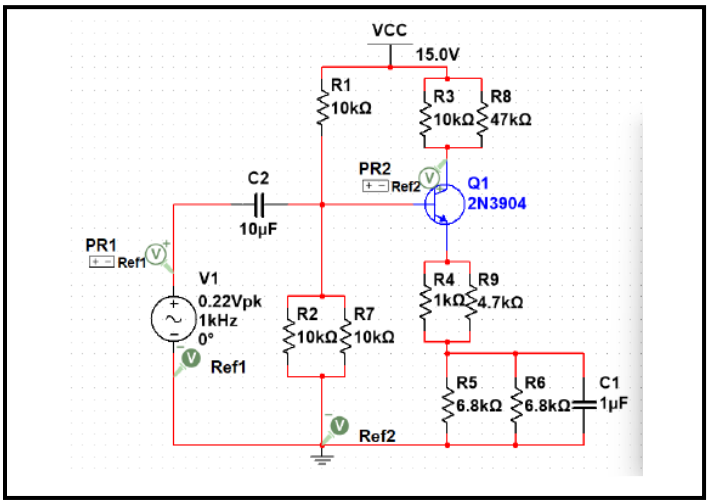

Fig. 10 BJT Common Emitter Amplifier Simulation Circuit

The simulation produced a peak-to-peak output voltage of 4.03 V, indicating successful signal amplification. Using the ratio of output to input voltage, the simulated voltage gain was calculated as:

$$A_V = -9.15V/V$$

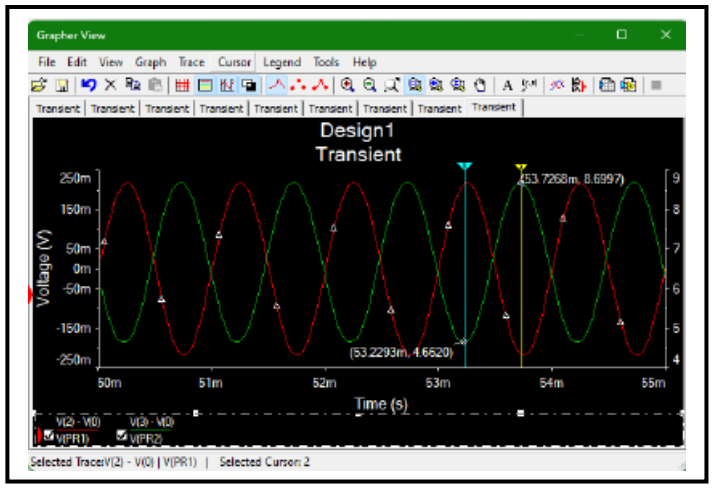

Fig. 11 BJT Common Emitter Simulation Oscilloscope Results.

This is slightly lower than the theoretical value of -10V/V, a discrepancy attributed primarily to the capacitive impedance and minor deviations in resistance due to parallel combinations. Capacitive reactance introduces frequency-dependent attenuation, particularly at lower signal frequencies.

The resulting percent error of approximately 8.5% falls within acceptable bounds for laboratory validation. This deviation is important to recognize, as similar or greater error margins may manifest in the hardware implementation due to component tolerances and non-ideal behavior.

For the hardware verification of the BJT-based common-emitter amplifier, the 2N3904 NPN transistor was employed. Special attention was paid to the correct identification and orientation of the transistor terminals—base, collector, and emitter—to ensure consistency with the simulation topology. The circuit was assembled using the calculated resistor values and configured identically to the simulation model.

After completion of the physical connections, DC bias voltages at the emitter (V_E), collector (V_C), and base (V_B) were measured using a digital multimeter in conjunction with the NI myDAQ data acquisition system. These values were compared to theoretical expectations to verify the integrity of the biasing network. Subsequently, an AC sinusoidal input signal of 0.44 V_{P-P} at 1 kHz was applied to the base via a coupling capacitor. Input and output waveforms were

observed on the oscilloscope to assess signal behavior through the amplifier.

Upon acquiring and analyzing the waveforms at 1 kHz, the input frequency was increased to 10KHz. The input amplitude was also adjusted to yield a target output of 4 V_{P-P}, consistent with design goals. This adjustment facilitated gain verification at higher frequencies and allowed further analysis of capacitive effects on amplifier performance.

Calculated vs Measured Common Emitter Amplifier Results.			
	Calculated	**Measured**	**Percent error**
V_B	5V	4.93V	1.4%
V_C	7V	6.52V	7.36%
V_E	3.3V	3.83V	16.06%
I_C	1.017mA	1.028mA	1.08%
A_V (f =1KHz) 0.44V_{PP}	-10V/V	-9.48V/V	5.2%
A_V (f = 10KHz) 0.44V_{PP}	-10V/V	-9.66V/V	3.4%

Fig. 12 Tabulated Common Emitter Amplifier results.

The experimental data confirmed successful implementation of the common-emitter amplifier. Using the measured collector voltage, the collector current was calculated as:

$$I_C = \frac{V_{CC} - V_C}{R_3} = \frac{15 - 6.52V}{8.246K\Omega} = 1.028mA$$

This value closely aligns with the design specification of I_C = 1mA, confirming proper current biasing. From the oscilloscope waveforms, the measured output voltage amplitudes were 4.169 V_{P-P} at 1 KHz and 4.252 V_{P-P} at 10 KHz. These slight deviations from the target 4 V_{P-P} output are primarily due to the input resolution limitations of the NI myDAQ function generator, which restricts amplitude control to two decimal places. Given the small input signal magnitude, this constraint becomes more pronounced. Nevertheless, the output remains within acceptable bounds for experimental verification.

Referring again to the comparative results table, all measured parameters are within reasonable proximity of their theoretical counterparts. The largest deviation was observed in the emitter voltage, likely caused by minor variations in resistance introduced by parallel combinations. While this deviation did not significantly impact the amplifier's gain, achieving tighter tolerances would require resistor values with lower percent error or precision trimming components. Despite component limitations, the amplifier successfully met all key design objectives: collector current (I_C) ≈ 1mA, collector voltage (V_C) ≈ 7V, and a base voltage V_B ≈ 5V.

VI. MOSFET VS BJT Amplifier

This study successfully demonstrated the implementation of two distinct single-stage amplifier configurations: a common-source amplifier utilizing an N-channel MOSFET and a common-emitter amplifier employing a BJT. Both architectures fulfill the fundamental role of voltage amplification; however, the choice between the two device types depends heavily on application-specific requirements.

The MOSFET, characterized by its extremely high input impedance, draws negligible input current. This property minimizes loading effects and makes it ideal for voltage buffer stages or circuits requiring minimal interaction with preceding stages—an advantage encountered in high-impedance sensor interfacing and analog switching. Additionally, MOSFETs exhibit superior switching speeds compared to BJTs, making them highly favorable in high-frequency and digital logic applications. Their simplified planar structure also allows for extreme scalability, an essential factor in VLSI (Very Large-Scale Integration) design.

In contrast, BJTs offer higher transconductance for a given bias current, which can yield greater gain in low-noise analog amplification. They are generally more robust in high-power applications and less prone to damage from electrostatic discharge due to their lack of delicate gate oxide layers. Moreover, BJTs tend to be more cost-effective, a factor worth considering in cost-sensitive designs.

While the MOSFET is more prevalent in modern electronics, particularly in integrated digital systems, the BJT remains relevant in scenarios

requiring high current drive, analog precision, or thermal stability.

In our experiments, both devices were used successfully to construct amplifiers meeting specified design targets. This reinforces the idea that neither device is inherently superior; rather, selection should be based on circuit requirements. Understanding the trade-offs between these technologies is essential to competent circuit design and ensures optimal performance across diverse electronic systems

VII. Conclusion

This project demonstrated a comprehensive exploration of transistor-based amplifier design through both theoretical analysis and practical implementation. By applying foundational concepts of biasing, gain estimation, and small-signal operation, we successfully designed and built two single-stage amplifiers: a Common Source (CS) amplifier using an N-channel MOSFET and a Common Emitter (CE) amplifier using an NPN BJT.

Design specifications were achieved by calculating appropriate component values and validating them through circuit simulation in NI Multisim. This simulation process ensured not only the accuracy of the designs but also the safety and feasibility of their physical construction. Upon successful verification, the circuits were implemented in hardware using components from a given component kit, and their performance was evaluated against expected parameters.

Measured values for bias points and output amplitudes closely matched calculated predictions, with minor deviations attributed to component tolerances, measurement limitations, and practical considerations such as resistor combinations. Both amplifier designs achieved their intended operating points and voltage gain, confirming the accuracy of the design methodology.

Finally, a comparison of the two semiconductor technologies highlighted the strengths and limitations of MOSFETs and BJTs. While each device offers specific advantages, selecting the appropriate component ultimately depends on the requirements of the intended application.

VIII. References

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